# SkSemAutom

## OUTCOME BASED CURRICULUM

Certificate Program on Practical Approach to SoC-Design

| Section | Section Name | Section Description | Lectures (Each Lecture is more than 30 mints) | Learning Objectives (After Completion of each lecture the Learner will be able to work on):- |
|---|---|---|---|---|
| Section-I | Practical Approach to SoC Design | ➢ This Section describes comprehensive overview of the SoC design process. It explains end-to-end system on chip (SoC) design processes and includes updated coverage of design methodology, the design environment, EDA tool flow, design decisions, choice of design intellectual property (IP) cores, sign-off procedures, and design infrastructure requirements.<br>➢ This Section also covers critical advanced guidance on the latest UPF-based low power design flow, challenges of deep submicron technologies, and 3D design fundamentals.<br>➢ This Section provides engineers who aspire to become VLSI designers with all the necessary information and details of EDA tools. | ➢ Introduction | ➢ Introduction to CMOS VLSI<br>➢ Application Areas of SoC<br>➢ Trends in VLSI<br>➢ System on Chip Complexity<br>➢ Integration Trend from Circuit to System on Chip<br>➢ Speed of Operation<br>➢ Die Size<br>➢ Design Methodology<br>➢ Skill Set Required<br>➢ EDA Environment<br>➢ Challenges in All |
| | | | ➢ System on Chip (SoC) Design<br>➢ Assessment | ➢ System on Chip (SoC)<br>➢ Constituents of SoC<br>➢ Application-Specific Processors<br>➢ Control Processors<br>➢ Digital Signal Processors<br>➢ Vector Processors<br>➢ SoC Development Life Cycle<br>➢ SoC Design Requirements<br>➢ Design Strategy<br>➢ SoC Design Planning<br>➢ System Modeling<br>➢ System Module Development Feasibility Study<br>➢ IP Design Decisions<br>➢ Verification Ips<br>➢ Target Technology Decision<br>➢ Development Plan<br>➢ EDA Tool Plan<br>➢ Design Center Infrastructure<br>➢ Computational Servers<br>➢ Filers<br>➢ Workstations<br>➢ Backup Servers<br>➢ Source Control Server<br>➢ Firewalls<br>➢ Resource Planning<br>➢ SoC Design Flow<br>➢ EVM Design Development Flow<br>➢ Software Development Flow<br>➢ Product Integration Flow |
| | | | ➢ SoC Constituents | ➢ SoC Constituents<br>➢ Issues of Hw-Sw Co-Design<br>➢ Embedded Memories<br>➢ Protocol Blocks<br>➢ Mixed Signal Blocks<br>➢ Radio Frequency (RF) Control Blocks<br>➢ Analog Blocks<br>➢ Third-Party IP Cores |

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| | | | | ➢ System Software<br>➢ GAMP Classification of Software<br>➢ Design-Specific Blocks |

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| Section-II | VLSI Logic Design and HDL | ➢ Basic logic functions are combinational and sequential circuits, but the majority of the SoC designs are sequential designs as it is easy to represent system functionality by data/control path architectures. This is easily done by defining their different states spread across time. Data path architectures of system definition can be extended to most of the subsystems if their functionality can be classified as a finite number of states. This requires identifying the system functionality as small logic partitions and realizing them as fundamental logic circuits. | ➢ VLSI Logic Design and HDL | ➢ SoC Design Concepts<br>➢ Asynchronous Circuits<br>➢ Speed Matching<br>➢ Network on Chip Architecture<br>➢ Hardware Accelerator<br>➢ Hardware Description Languages (HDL<br>➢ Behavioral Modelling of the Hardware System<br>➢ Dataflow Modeling of the Hardware System<br>➢ Structural Modeling of the Hardware System<br>➢ Input-Output Pad Instantiation |
| | | | ➢ Synthesis and Static Timing Analysis (STA) | ➢ SoC Synthesis<br>➢ Design Rule Constraints<br>➢ SoC Design Synthesis<br>➢ Low-Power Synthesis<br>➢ Reports<br>➢ Static Timing Analysis (STA)<br>➢ Timing Definition<br>➢ Timing Delay Calculation Concepts<br>➢ Timing Analysis<br>➢ Modeling Process, Voltage, and Temperature Variations<br>➢ Timing and Design Constraints<br>➢ Organizing Paths to Groups<br>➢ Design Corners<br>➢ Challenges of STA During SoC Design |
| | | | ➢ SoC Design Verification | ➢ Importance of Verification<br>➢ Verification Plan and Strategies<br>➢ Verification Plan<br>➢ Functional Verification<br>➢ Verification Methods<br>➢ Design for Verification<br>➢ Verification Example<br>➢ Verification Tools<br>➢ Verification Language<br>➢ Automation Scripts<br>➢ Design for Verification<br>➢ Assertions in Verification<br>➢ Verification Reuse and Verification Ips<br>➢ Universal Verification Methodology (UVM)<br>➢ Bug and Debug<br>➢ Bug Tracking Workflow<br>➢ FPGA Validation<br>➢ Validation on Development Boards |

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| Section-III | SoC Physical Design | ➢ VLSI SoC design flow involves stages where the design is converted to different forms until the time it is taped out for fabrication. These design conversions are from the design requirements or specification in document format to register transfer level (RTL) as behavioural model to design netlist in structural form (gate-level) to design layout as physical structures. | ➢ SoC Physical Design | ➢ Re-convergent Model of VLSI SoC Design<br>➢ File Formats<br>➢ SoC Physical Design<br>➢ Physical Design Theory<br>➢ Stick Diagrams<br>➢ Physical Design Setup and Floor Plan<br>➢ Floor Planning<br>➢ SoC Power Plan<br>➢ Two-Step Synthesis of SoC Design<br>➢ Placement<br>➢ Physical Design Constraints<br>➢ Clock Tree Synthesis (CTS)<br>➢ Routing<br>➢ ECO Implementation<br>➢ Advanced Physical Design of SoCs<br>➢ Photolithography and Mask Pattern |
| | | | ➢ SoC Physical Design Verification | ➢ SoC Design Verification by Formal Verification<br>➢ Model Checking<br>➢ Logic Equivalence Check (LEC)<br>➢ Static Timing Analysis (STA)<br>➢ ECO Checks<br>➢ Electromigration (EM)<br>➢ Simultaneous Switching Noise (SSN)<br>➢ Electrostatic Discharge (ESD) Protection<br>➢ IR and Cross Talk Analysis<br>➢ Layout Verse Schematic (LVS)<br>➢ Gate Level Simulation<br>➢ Electrical Rule Check (ERC)<br>➢ DRC Rule Check<br>➢ Design Rule Violation (DRV) Checks<br>➢ Design Tape Out |

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| Section-IV | SoC Packaging & Reference Designs | ➢ VLSI SoCs have to be packaged such that they can interface with the rest of the world in a product to be used as a single unit or be interfaced with other circuits. They also have to be protected from mechanical stress, environment (humidity, pollution), and electrostatic discharge during handling. In addition, SoCs have to be exposed to be tested to ensure reliability with tests like the environmental test, burn-in tests, and other safety tests before they are ready for use. This is achieved by packaging it. Packaging provides a high-yield assembly for the next level of integration or interconnection on board for realizing the final product. Hence, the package must meet all device performance requirements such as electrical (inductance, capacitance, cross talk), thermal (power dissipation, junction temperature), quality, reliability, cost objectives, and testability at the package level. Hence, system on chip dies are assembled in the package. | ➢ SoC Packaging | ➢ Introduction to VLSI SoC Packaging<br>➢ Classification of Packages<br>➢ Criteria for Selection of Packages<br>➢ Package Components<br>➢ Package Assembly Flow<br>➢ Packaging Technology<br>➢ Flip-Chip Packages<br>➢ Typical Packages<br>➢ Package Performance<br>➢ System Integration<br>➢ Packaging Trends |
| | | | ➢ Reference Designs | ➢ Design for Trial<br>➢ Prerequisites<br>➢ User Guidelines<br>➢ Design Directory<br>➢ Arithmetic functions<br>➢ Logical function blocks<br>➢ Design Examples<br>➢ Design Flow<br>➢ Logic Equivalence Check (LEC)<br>➢ MINI-SoC Design |
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| Section-V | AMBA Design | ➢ This section introduces the main features of Advanced Microcontroller Bus Architecture (AMBA) AXI4, highlighting the differences from the previous version AXI3. The section explains the key concepts and details that help you implement the AXI4 protocol. | ➢ AMBA | ➢ What is AMBA, and why use it?<br>➢ Where is AMBA used?<br>➢ Why use AMBA?<br>➢ How has AMBA evolved? |
| | | | ➢ AXI protocol | ➢ AXI in a multi-master system<br>➢ AXI channels<br>➢ Main AXI features |
| | | | ➢ Channel transfers and transactions | ➢ Channel handshake<br>➢ Differences between transfers and transactions<br>➢ Channel transfer examples<br>➢ Write transaction: single data item<br>➢ Write transaction: multiple data items<br>➢ Read transaction: single data item<br>➢ Read transaction: multiple data items<br>➢ Active transactions |
| | | | ➢ Channel signals<br>➢ Atomic Process | ➢ Write channel signals<br>➢ Read channel signals<br>➢ Data size, length, and burst type<br>➢ Protection level support<br>➢ Cache support<br>➢ Response signaling<br>➢ Write data strobes<br>➢ Atomic accesses with the lock signal<br>➢ Quality of service<br>➢ Region signaling<br>➢ User signals<br>➢ AXI channel dependencies<br>➢ Locked accesses<br>➢ Exclusive accesses<br>➢ Exclusive access hardware monitor operation<br>➢ Exclusive transaction pairs: both pass<br>➢ Exclusive transaction pairs: one pass, one fail |
| | | | ➢ Transfer behavior and transaction ordering | ➢ Examples of simple transactions<br>➢ Transfer IDs<br>➢ Write transaction ordering rules<br>➢ Read transaction ordering rules<br>➢ Read and write channel ordering<br>➢ Unaligned transfer start address<br>➢ Endianness support<br>➢ Read and write interface attributes<br>➢ Project on AHB design |

Note: Eligibility: M.Tech/ME/B.Tech/BE/MSc/BSc (Complited/Pursuing) (ECE/EEE/Electronics/Computer Science)
Placement: - Complete Assistance provided after End-Exam Qualify.
Duration: - 12 Weeks through Online Classes
Fees: - Rs 6000/-

# Thank You